Please replace the paragraph on page 21, lines 9-15 with the following amended paragraph.

In the Figure 7B embodiment, processor A 752 or processor B 770 may execute the overhead code identified in step 652 and created as object files in step 672 of the Figure 6 process. DSP 0 756, DSP 1 758, and DSP 2 760 may execute the kernel code identified in step 652. Each processing element processor A ~~702~~ 752 and processor B ~~720~~ 770 is supplied with an instruction port, instruction port ~~724~~ 774 and instruction port ~~722~~ 772, respectively, for fetching instructions for execution of overhead code.

Please replace the paragraph on page 26, lines 6-8 with the following amended paragraph.

In the exemplary Figure 9C emobodiment, RTK 704 loads the first overhead code 910, ~~960~~ 950 sections into processor 1 702 and processor B 720, respectively, for execution in time periods 980 and 962, respectively.

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Please replace the paragraph on page 26, lines 6-8 with the following amended paragraph.

In Figure 10 embodiment, it should be noted that it is not necessary that there be an valid entry at each location of the matrix. There are situations where there are relatively few valid sets of designs, bins, and ~~varients~~ variants. These situations give rise to a sparsely-populated TAPR matrix. In other situations, there may be a valid set of designs, bins and ~~varients~~ variants for all locations in the matrix. These situations give rise to a fully-populated TAPR matrix.